PRELIMINARY AMENDMENT

Please amend the above-referenced patent application as follows:

In the Claims:

Please amend claims 1-2, 5, 7-8, 10, 12-13, and 15. Please add new claim 20. Currently pending claims 1-20 for consideration by the Examiner are as follows:

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12 = 2f 1. (currently amended) A method of testing a semiconductor chip having a plurality of common I/Os associated therewith whose characteristics or properties may be tested by applying a test signal through a control I/O, the method comprising the steps of:

performing connectivity testing a chip-to-package ~~connectivity test upon~~ connection of at least one of the common I/O through the control I/O; and

determining whether the ~~common I/O~~ chip-to-package connection is faulty from a result of the ~~chip-to-package~~ connectivity testing.

2. (currently amended) The method of claim 1, wherein ~~performing a pin-to-package~~ the connectivity testing comprises:

launching a transition signal through the common I/O to an associated I/O package connection and pad; and

observing a response of the transition.

3. (original) The method of claim 2, further comprising: triggering a first latch at an initialization

of the transition response and triggering a second latch when the transition response has reached a transition threshold value.

4. (original) The method of claim 3, wherein determining whether the chip-to-package connection is faulty comprises: comparing a difference between values stored in association with the first and second latches.

5. (currently amended) The method of claim 1, wherein determining whether the chip-to-package connection is faulty comprises: comparing a first RC constant associated with a first signal relating to a connectivity testing of a first I/O with a second RC constant associated with a second signal relating to a connectivity testing of a second I/O.

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6. (original) The method of claim 5, further comprising identifying the first I/O as having a faulty connection if the first RC constant is greater than the second RC constant.

7. (currently amended) The method of claim 1, wherein performing ~~the chip-to-package~~ connectivity testing comprises generating a transition signal from a driver of the common I/O, wherein the driver is configured as a weak driver.

8. (currently amended) The method of claim 7, wherein ~~generating the transition from the weak driver comprises~~ further comprising placing an additional impedance into connection with the driver prior to ~~launching~~ generating the transition signal.

9. (original) The method of claim 8, wherein placing an additional impedance into connection with the driver comprises placing a resistor into series connection with the driver.

10. (currently amended) The method of claim 8, further comprising electrically shorting the additional impedance from connection with the driver after ~~launching~~ generating the transition signal.

11. (original) The method of claim 10, wherein electrically shorting the additional impedance includes completing a circuit around the additional impedance to bypass the additional impedance.

12. (currently amended) A method of reduced pin count testing the chip-to-package connectivity of a semiconductor device, the method comprising:

launching a transition signal from a common I/O driver on the packaged semiconductor device;

observing a response of the transition signal at a point within the semiconductor device;

determining whether a chip-to-package connection associated with the I/O is faulty from the response of the transition signal.

13. (currently amended) The method of claim 12, further comprising driving the transition signal with a weak driver.

14. (original) An apparatus configured to launch a test signal to a common I/O of a semiconductor device from a driver on the semiconductor device which is associated with the common I/O using reduced pin count testing, the apparatus comprising:

a test fixture configured to couple to the common I/O of the semiconductor device;

a weak driver impedance coupled between the driver and the test fixture;

wherein the apparatus is configured to launch the test signal through the weak driver impedance and the common I/O to the test fixture and evaluate a characteristic of a response to the test signal to determine whether a chip-to-package connection associated with the common I/O is faulty.

15. (currently amended) The apparatus of claim 14, wherein the weak driver impedance includes ~~at least one of~~ a switchable impedance ~~and a variable impedance~~.

16. (original) The apparatus of claim 14, wherein the weak driver impedance is an impedance having a resistive value of 1 KΩ or more.

17. (original) The apparatus of claim 16, wherein the weak driver impedance is approximately 10 KΩ or more.

18. (original) The apparatus of claim 14, further comprising a fixture impedance coupled between the test fixture and at least one of the semiconductor device and a potential relative to the semiconductor device.